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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,241	12/31/2003	Jeong Ho Park	09407.0001	6968
22852	7590	11/24/2006	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413				ISAAC. STANETTA D
ART UNIT		PAPER NUMBER		
		2812		

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,241	PARK, JEONG HO	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 21 September 2006.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 13-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 13-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 11 July 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the amendment filed on 9/21/06. Currently, claims 13-23 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park US Patent 6,642,130 in view of Kim US Patent 6,534,352.

Park discloses the semiconductor method substantially as claimed. See figures 1-8, and corresponding text, where Park shows, pertaining to claim 13, a method for fabricating a semiconductor transistor, comprising: forming a first insulating layer **18** on a substrate **11** (figure 4; col. 3, lines 27-30); performing an ion implantation for forming a lightly-doped drain (LDD) region **15** in the substrate (figure 2; col. 3, lines 8-15); patterning the first insulating layer (figure

4; col. 3, lines 27-30); forming a trench in the substrate, the trench **C** extending through the first insulating layer and the LDD region, and the trench extending into a portion of the substrate (figure 4; col. 3, lines 28-35); forming a trench gate **21** by depositing a second insulating layer **20**, and depositing and planarizing a conductor **21** on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor, wherein the trench gate is formed after forming the LDD region (figure 6; col. 3, lines 60-66); anisotropically etching the first insulating layer to form spacers **18**(figure 5; col. 3, lines 37-43); and forming source/drain regions **16** by performing an ion implantation on the substrate, wherein the source/drain regions are formed after forming the LDD region (figure 1; col. 3, lines 10-15). In addition, Park shows, pertaining to claim 14, further comprising performing a thermal process after forming the source/drain regions. Also, Park shows, pertaining to claim 15, wherein the first insulating layer is an oxide layer or a nitride layer (col. 3, lines 28-30, oxide layer). Park shows, pertaining to claim 16, wherein the conductor comprises one selected from the group consisting of polysilicon, tungsten alloys, titanium alloys, and tantalum alloys (col. 3, lines 60-64). Finally, Park shows, pertaining to claim 19, wherein the trench is formed by dry etching (col. 3, lines 16-18 and lines 40-48).

However, Park fails to show, pertaining to claim 13, forming a trench gate by planarizing a second insulating layer. In addition, Park fails to show, pertaining to claim 17, wherein the energy of the ion implantation for forming the LDD regions is between 10 keV and 80 keV. Also, Park fails to show, pertaining to claim 18, wherein the energy of the ion implantation for forming the source/drain regions is between 10 keV and 100 keV. Park fails to show, pertaining to claim 20, wherein the trench is formed by a dry etch using an angle etching and chemical dry

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etching. In addition, Park fails to show, pertaining to claim 21, wherein lower edges of the trench are formed in a round shape. Also, Park fails to show, pertaining to claim 22, wherein the chemical dry etching uses CF_4/O_2 or CHF_3/O_2 . Finally, Park fails to show, pertaining to claim 23, wherein planarizing a second insulating layer and a conductor comprises a CMP process using the first insulating layer as an etch-stop layer.

Kim teaches, a similar method of forming a trench gate by planarizing the gate insulating layer (implied second insulating layer) and conductor material while using the first insulating layer as an etch-stop layer (figures 2G and 2H; col. 5, lines 5-22).

It would have been obvious to one of ordinary skill in the art to substitute, forming a trench gate by planarizing a second insulating; wherein planarizing a second insulating layer and a conductor comprises a CMP process using the first insulating layer as an etch-stop layer, in the method of Park, pertaining to claims 13 and 23, according to the teachings of Kim with the motivation that, both Park and Kim teach the formation of a trench gate for a highly integrated MOSFET transistor device. In addition, both Park and Kim teach the second insulating layer to be the gate insulating layer for the trench gate. Therefore, the second insulating layers, as taught by both Park and Kim, would prove to have equivalent device functions, since ultimately the goal is to create a conventional gate insulating layer for the trench gate. Also, one of ordinary skill in the art would be drawn to planarizing the second insulating film for the purpose of lowering the resistance of the highly integrated MOSFET transistor device, resulting in a more efficient semiconductor device.

It would have been obvious to one of ordinary skill in the art to incorporate the following steps of: wherein the energy of the ion implantation for forming the LDD regions is between 10

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keV and 80 keV; wherein the energy of the ion implantation for forming the source/drain regions is between 10 keV and 100 keV; wherein the trench is formed by a dry etch using an angle etching and chemical dry etching; wherein lower edges of the trench are formed in a round shape; wherein the chemical dry etching uses CF₄/O₂ or CHF₃/O₂, in the method of Park, pertaining to claims 17, 18 and 20-22, according to both the teachings of Park in view of Kim, with the motivation that having the desired energy of the ion implantation process for LDD regions and source/drain regions would result in routine experimentation, where one of ordinary skill in the art would be able to adjust the amount of energy produced to create a desired LDD and source/drain regions. In addition, forming a trench by dry etching is well known to one of ordinary skill in the art, where dry etching is attractive for creating a trench wall profile, hence would also result in routine experimentation.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park US Patent 6,642,130 in view of Kim US Patent 6,534,352 in further view of, Li et al., US Patent 6,309,933.

Park in view of Kim discloses the semiconductor method substantially as claimed. See preceding rejection.

However, Park in view of Kim fails to show, using the spacers and the trench gate as a mask to form the source/drain regions.

Li teaches, a similar method of forming a trench gate where the spacers and the trench gate are used as a mask to form the source/drain regions (figures 17 and 19; col. 6, lines 63-67; col. 7, lines 7-12).

It would have been obvious to one of ordinary skill in the art to incorporate, using the spacers and the trench gate as a mask to form the source drain regions, in the method of Park in view of Kim, pertaining to claim 13, according to the teachings of Li, with the motivation that by using the spacers and the trench gate as a mask, the ion implantation process used to form the source/drain regions would be performed with great precision and accuracy, allowing for a more efficient semiconductor device.

Response to Arguments

Applicant's arguments with respect to claims 13-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

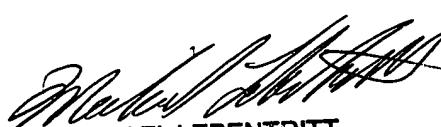
however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
November 20, 2006



MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER